1. A magnetic memory comprising:

a plurality of bit lines;

a plurality of word lines crossing the bit lines;

a plurality of magnetic memory elements disposed at intersections of the bit lines and the word lines, each of the memory cells comprising a free layer with reversible magnetization and a pinned layer with fixed magnetization;

a reference potential generating circuit configured to generate a predetermined reference potential;

a write bit line current controlling circuit configured to control write bit line current passing through the bit lines in a write operation on the basis of a reference potential generated by the reference potential generating means; and

a write word line current controlling circuit configured to control write word line current passing through the word lines in the write operation on the basis of a reference potential generated by the reference potential generating circuit.

2. The magnetic memory of Claim 1, wherein

the write bit line current controlling circuit includes a first transistor having a gate for receiving the reference potential to pass the write bit line current, and

the write word line current controlling circuit includes a second transistor having a gate for receiving the reference potential to pass the write word line current.

HN 9/30/05

3. The magnetic memory of Claim ~~3~~ 2, wherein

a ratio of a channel width/channel length of the first transistor to a channel width/channel length of the second transistor is set to be substantially equal to a ratio of the write bit line current to the write word line current.